1. An integrated circuit capacitor comprising:

a first electrode and a second electrode formed on a substrate; and

a dielectric provided between said electrodes, said capacitor having a first lower section formed in a first insulating layer and a second upper section formed in a second insulating layer, said first lower section being formed beneath said second upper section and wherein said upper section has a width greater than said lower section.

2. The integrated circuit capacitor according to claim 1, wherein said capacitor is a container capacitor.

3. The integrated circuit capacitor according to claim 1, wherein said first electrode and second electrode are independently formed of a material selected from doped polysilicon, hemispherical grained polysilicon or a metal.

4. The integrated circuit capacitor according to claim 3, wherein said first electrode is formed of hemispherical grained polysilicon.

5. The integrated circuit capacitor according to claim 3, wherein said second electrode is formed of doped polysilicon.

6. The integrated circuit capacitor according to claim 1, wherein said dielectric is selected from the group consisting of oxides and nitrides.

7. The integrated circuit capacitor according to claim 6, wherein said dielectric is an oxide selected from the group consisting of $Ta_2O_5$, $SrTiO_3$, $Y_2O_3$, $Nb_2O_5$, $ZrO_2$, titanium oxide, and silicon nitride.

8. The integrated circuit capacitor according to claim 1, wherein said capacitor is a stacked capacitor.

9. The integrated circuit capacitor according to claim 1, wherein said first electrode is in direct contact with an active area of said substrate.

10. The integrated circuit capacitor according to claim 1, wherein said capacitor is part of a DRAM cell.

11. A computer system comprising:

a processor; and

a memory circuit connected to the processor, wherein at least one of said processor and memory circuit contains at least one capacitor formed on a substrate having a first electrode and a second electrode with a dielectric layer provided between said electrodes, said capacitor having a first lower section formed in a first insulating layer and a second upper section formed in a second insulating layer, said first lower section being formed beneath said second upper section and wherein said upper section has a width greater than said lower section.

12. The computer system according to claim 11, wherein said capacitor is a container capacitor.

13. The computer system according to claim 11, wherein said first electrode and second electrode are independently formed of a material selected from doped polysilicon, hemispherical grained polysilicon or a metal.

14. The computer system according to claim 13, wherein said first electrode is formed of hemispherical grained polysilicon.

15. The computer system according to claim 13, wherein said second electrode is formed of doped polysilicon.

16. The computer system according to claim 11, wherein said dielectric is selected from the group consisting of oxides and nitrides.

17. The computer system according to claim 16, wherein said dielectric is an oxide selected from the group consisting of $Ta_2O_5$, $SrTiO_3$, $Y_2O_3$, $Nb_2O_5$, $ZrO_2$, titanium oxide, and silicon nitride.

18. The computer system according to claim 11, wherein said capacitor is a stacked capacitor.

19. The computer system according to claim 11, wherein said first electrode is in direct contact with an active area of said substrate.

20. The computer system of claim 11, wherein said memory circuit is a DRAM memory circuit.

21. A memory cell comprising:

a transistor; and

a capacitor formed on a substrate having a first electrode and a second electrode with a dielectric layer provided between said electrodes, said transistor and capacitor being connected in a memory array, said capacitor having a first lower section formed in a first insulating layer and a second upper section formed in a second insulating layer, said first lower section being formed beneath said second upper section and wherein said upper section has a width greater than said lower section.

22. The memory cell according to claim 21, wherein said capacitor is a container capacitor.

23. The memory cell according to claim 21, wherein said first electrode and second electrode are independently formed of a material selected from doped polysilicon, hemispherical grained polysilicon or a metal.

24. The memory cell according to claim 23, wherein said first electrode is formed of hemispherical grained polysilicon.

25. The memory cell according to claim 23, wherein said second electrode is formed of doped polysilicon.

26. The memory cell according to claim 21, wherein said dielectric is selected from the group consisting of oxides and nitrides.

27. The memory cell according to claim 21, wherein said capacitor is a stacked capacitor.

28. The memory cell according to claim 21, wherein said first electrode is in direct contact with an active area of said substrate.

29. The memory cell according to claim 21, wherein said integrated circuit is a DRAM cell.

30. A DRAM cell having a container capacitor, said capacitor comprising:

a first electrode and a second electrode formed on a substrate; and

a dielectric provided between said electrodes, said capacitor having a first lower section formed in a first insulating layer and a second upper section formed in a second insulating layer, said first lower section being formed beneath said second upper section and wherein said upper section has a width greater than said lower section.

31. The DRAM cell according to claim 30, wherein said capacitor is a container capacitor.

32. The DRAM cell according to claim 30, wherein said first electrode and second electrode are independently formed of a material selected from doped polysilicon, hemispherical grained polysilicon or a metal.

33. The DRAM cell according to claim 32, wherein said first electrode is formed of hemispherical grained polysilicon.

34. The DRAM cell according to claim 32, wherein said second electrode is formed of doped polysilicon.

35. The DRAM cell according to claim 30, wherein said dielectric is selected from the group consisting of oxides and nitrides.

36. The DRAM cell according to claim 30, wherein said capacitor is a stacked capacitor.

37. The DRAM cell according to claim 30, wherein said first electrode is in direct contact with an active area of said substrate.

38. The DRAM cell according to claim 30, wherein said integrated circuit is a DRAM cell.

39. A method for fabricating an integrated circuit capacitor comprising:

forming a container opening in a first insulating layer formed over a substrate;

forming an oxide layer over said substrate in said container opening;

forming a plug over said oxide layer;

forming a second insulating layer over said conductive plug and said first insulating layer;

etching said second insulating layer such that the space formed in said second insulating layer is wider than said plug;

removing said plug and said oxide layer to form a container opening;

forming a first conductive layer in said container opening over an active area of said substrate;

forming a first dielectric layer atop said first conductive layer; and

forming a second conductive layer atop said dielectric layer.

40. The method according to claim 39, wherein said first and second insulating layer are selected from borophosphosilicate glass (BPSG), phososilicate glass (PSG), borosilicate glass (BSG) and undoped $SiO_2$.

41. The method according to claim 40, wherein said first and second insulating layers are formed of BPSG.

42. The method according to claim 39, wherein said oxide is formed by a wet chemical process.

43. The method according to claim 42, wherein said wet chemical process includes ozone treatment.

44. The method according to claim 42, wherein said wet chemical process includes an oxidation process.

45. The method according to claim 39, wherein said second insulating layer is etched with a selective etch.

46. The method according to claim 45, wherein said selective etch is a dry etch.

47. The method according to claim 39, wherein said plug is removed by selective etching with an aqueous TMAH solution.

48. The method according to claim 47, wherein said aqueous TMAH solution includes from about 0.5% to about 5% by volume TMAH.

49. The method according to claim 48, wherein said aqueous TMAH solution includes about 2.25% by volume TMAH.

50. The method according to claim 39, wherein said first and second conductive layers are independently formed of a material selected from doped polysilicon, hemispherical grained polysilicon or a metal.

51. The method according to claim 50, wherein said first conductive layer is formed of hemispherical grained polysilicon.

52. The method according to claim 50, wherein said second conductive layer is formed of doped polysilicon.

53. The method according to claim 39, wherein said dielectric layer is selected from the group consisting of oxides and nitrides.

54. The method according to claim 39, wherein said first conductive layer is in direct contact with an active area in said substrate.

55. A method for fabricating a DRAM cell container capacitor comprising:

forming a container opening in a first insulating layer formed over a substrate;

forming an oxide layer over said substrate;

forming a plug over said oxide layer;

forming a second insulating layer over said plug and said first insulating layer;

etching said second insulating layer such that the space formed in said second insulating layer is larger than said plug;

removing said plug and said oxide layer to form a container opening;

forming a first conductive layer in said container opening over an active area of said substrate;

forming a first dielectric layer atop said first conductive layer; and

forming a second conductive layer atop said dielectric layer.

56. The method according to claim 55, wherein said capacitor is a container capacitor.

57. The method according to claim 55, wherein said first conductive layer and second conductive layer are independently formed of a material selected from doped polysilicon, hemispherical grained polysilicon or a metal.

58. The method according to claim 57, wherein said first conductive layer is formed of hemispherical grained polysilicon.

59. The method according to claim 57, wherein said second conductive layer is formed of doped polysilicon.

60. The method according to claim 55, wherein said dielectric layer is selected from the group consisting of oxides and nitrides.

61. The method according to claim 55, wherein said capacitor is a stacked capacitor.

62. The method according to claim 55, wherein said integrated circuit is a DRAM cell.

63. The method according to claim 55, wherein said first conductive layer is in direct contact with an active area in said substrate.

64. A capacitor structure formed by the method comprising:

forming a container opening in a first insulating layer formed over a substrate;

forming an oxide layer over said substrate;

forming a plug over said oxide layer;

forming a second insulating layer over said plug and said first insulating layer;

etching said second insulating layer such that the space formed in said second insulating layer is wider than said plug;

removing said plug and said oxide layer to form a container opening;

forming a first conductive layer in said container opening over an active area of said substrate;

forming a first dielectric layer atop said first conductive layer; and

forming a second conductive layer atop said dielectric layer.

65. The capacitor structure according to claim 64, wherein said capacitor is a container capacitor.

66. The capacitor structure according to claim 64, wherein said first conductive layer and second conductive layer are independently formed of a material selected from doped polysilicon, hemispherical grained polysilicon or a metal.

67. The capacitor structure according to claim 66, wherein said first conductive layer is formed of hemispherical grained polysilicon.

68. The capacitor structure according to claim 66, wherein said second conductive layer is formed of doped polysilicon.

69. The capacitor structure according to claim 64, wherein said dielectric layer is selected from the group consisting of oxides and nitrides.

70. The capacitor structure according to claim 69, wherein said dielectric layer is selected from the group consisting of $Ta_2O_5$, $SrTiO_3$, $Y_2O_3$, $Nb_2O_5$, $ZrO_2$, titanium oxide, and silicon nitride.

71. The capacitor structure according to claim 64, wherein said capacitor is a stacked capacitor.

72. The capacitor structure according to claim 64, wherein said first conductive layer is in direct contact with an active area in said substrate.

73. The capacitor structure according to claim 64, wherein said integrated circuit is a DRAM cell.

74. A method for fabricating an integrated circuit capacitor comprising:

providing a first insulating layer formed over a substrate having a first opening;

providing a second insulating layer over said first insulating layer having a second opening which has a greater width than said first opening;

forming a first conductive layer over said container openings;

forming a first dielectric layer atop said first conductive layer; and

forming a second conductive layer atop said dielectric layer.

75. The method according to claim 74, wherein said capacitor is a container capacitor.

76. The method according to claim 74, wherein said first conductive layer and said second conductive layer are independently formed of a material selected from doped polysilicon, hemispherical grained polysilicon or a metal.

77. The method according to claim 76, wherein said first conductive layer is formed of hemispherical grained polysilicon.

78. The method according to claim 76, wherein said second conductive layer is formed of doped polysilicon.

79. The method according to claim 74, wherein said dielectric layer is selected from the group consisting of oxides and nitrides.

80. The method according to claim 74, wherein said capacitor is a stacked capacitor.

81. The method according to claim 74, wherein said first conductive layer is in direct contact with an active area in said substrate.